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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,674	12/29/2000	Paolo Faraboschi	00-BN-059 (STMI01-00059)	9124

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EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/751,674	FARABOSCHI ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 have been considered. Claims 1, 5, 8-10, 14, and 17-22 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 11 July 2005.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller et al., U.S. Patent Number 5,819,058 (herein referred to as Miller) in view of Jouppi, U.S. Patent Number 6,167,503 (herein referred to as Jouppi).

5. Referring to claims 1 and 10, taking claim 10 as exemplary, Miller has taught a processing system comprising:

a. A data processor (Miller column 3, lines 52-64 and Figure 1);

b. A memory coupled to said data processor (Miller column 3, lines 52-64 and Figure 1); and

c. A plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor (Miller column 3, lines 52-64 and Figure 1);

d. Wherein said data processor comprises:

i. An instruction execution pipeline having a plurality of processing stages (Miller column 3, lines 18-19 and Figure 1) capable of executing instruction bundles each comprising one or more syllables (Miller column 4, line 38 to column 5, line 8 and Figure 2), wherein each of said instruction execution pipelines is a plurality of lanes wide (Miller column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6), each of said lanes capable of receiving one or more of said syllables of said instruction bundles (Miller column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6). In regards to Miller, lanes are defined by the execution units, since the path to an execution unit creates a lane, i.e. the lane leads to a specific execution unit. Therefore, the paths to the execution units, e.g. the ALU, MUL, RCU, etc., in Miller are lanes.

ii. An instruction cache capable of storing a plurality of cache lines (Miller column 9, lines 16-36; column 10, lines 36-59; and Figure 7), each of said cache lines comprising a plurality of the syllables (Miller column 9, lines 16-36; column 10, lines 36-59; and Figure 7);

iii. An instruction issue unit capable of receiving fetched ones of said plurality of cache lines and issuing complete instruction bundles toward said execution clusters (Miller column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6),

wherein at least one complete instruction bundle is issued having an out-of-order alignment (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6); and

iv. Alignment and dispersal circuitry capable of receiving said complete instruction bundles from said instruction issue unit and routing each of said received complete instruction bundles to a correct one of said execution clusters (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6) as a function of at least one address bit associated with each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B), the alignment and dispersal circuitry also capable of reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6).

6. Miller has not taught a plurality of execution clusters. Jouppi has taught a plurality of execution clusters (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B). A person of ordinary skill in the art at the time the invention was made, and as taught by Jouppi, would have recognized that the clusters of Jouppi increases the number of instruction concurrently issued without

substantially increasing the complexity of the interconnects to the registers (Jouppi column 1, line 66 to column 2, line 3), thereby increasing parallelism and efficiency without increasing circuit complexity. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the execution clusters of Jouppi in the device of Miller to increase processor parallelism and efficiency without increasing the circuit complexity.

7. Claim 1 has similar limitations to claim 10 and is rejected under the same grounds as claim 1 above. Claim 1 differs in that it is a data processor instead of a processing system as in claim 10, so it does not have the limitations of memory coupled to the processor and peripheral circuits.

8. Referring to claims 2 and 11, Miller in view of Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of at least one address bit associated with at least one syllable in each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B).

9. Referring to claims 3 and 12, Miller in view of Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a cluster bit associated with each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B).

10. Referring to claims 4 and 13, Miller in view of Jouppi has taught wherein said alignment and dispersal circuitry routes each of said received complete instruction bundles to said correct execution cluster as a function of a stop bit associated with at least

one syllable in each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B).

11. Referring to claims 5 and 14, Miller in view of Jouppi has taught wherein said alignment and dispersal circuitry comprises multiplexer circuitry capable of routing each of said received complete instruction bundles to any one of said execution clusters (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6).

12. Referring to claims 6 and 15, Miller in view of Jouppi has taught wherein said alignment and dispersal circuitry comprises control logic circuitry capable of controlling said multiplexer circuitry (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6).

13. Referring to claims 7 and 16; Miller in view of Jouppi has taught wherein said control logic circuitry controls said multiplexer circuitry as a function of at least one of:

a. Said at least one address bit associated with each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B);

b. At least one address bit associated with at least one syllable in each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B); and

c. A cluster bit associated with each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B).

14. Referring to claims 8 and 17, Miller in view of Jouppi has taught wherein each execution pipeline is four lanes wide (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6).

15. Referring to claims 9 and 18, Miller in view of Jouppi has taught wherein the data processor comprises three execution units (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6).

16. Referring to claim 19, Miller has taught an instruction execution pipeline having a plurality of processing stages (Miller column 3, lines 18-19 and Figure 1) capable of executing instruction bundles each comprising one or more syllables (Miller column 4, line 38 to column 5, line 8 and Figure 2), wherein each of said instruction execution pipelines is a plurality of lanes wide (Miller column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6), each of said lanes capable of receiving one or more of said syllables of said instruction bundles (Miller column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6). In regards to Miller, lanes are defined by the execution units, since the path to an execution unit creates a lane, i.e. the lane leads to a specific execution unit. Therefore, the paths to the execution units, e.g. the ALU, MUL, RCU, etc., in Miller are lanes. A method of routing instruction bundles into the lanes in the execution clusters comprising the steps of:

a. Fetching cache lines from an instruction cache, each of the cache lines comprising a plurality of the syllables (Miller column 9, lines 16-36; column 10, lines 36-59; and Figure 7);

b. Issuing complete instruction bundles toward the execution clusters, wherein at least one complete instruction bundle is issued having an out-

of-order alignment (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6);

c. Reordering each of the at least one complete instruction bundle having the out-of-order alignment so as to align the syllables in the complete instruction bundle with correct ones of the lanes (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6); and

d. Routing each of the complete instruction bundles to a correct one of the execution clusters as a function of at least one of:

i. At least one address bit associated with each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B);

ii. At least one address bit associated with at least one syllable in each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B); and

iii. A cluster bit associated with each of said complete instruction bundles (Miller column 5, line 9 to column 6, line 52; Figure 3A; and Figure 3B).

17. Miller has not taught a plurality of execution clusters. Jouppi has taught a plurality of execution clusters (Jouppi Abstract, lines 8-9; column 2, lines 22-30; column 4, lines 25-38; Figure 2A; and Figure 2B). A person of ordinary skill in the art at the time the invention was made, and as taught by Jouppi, would have recognized that the

clusters of Jouppi increases the number of instruction concurrently issued without substantially increasing the complexity of the interconnects to the registers (Jouppi column 1, line 66 to column 2, line 3), thereby increasing parallelism and efficiency without increasing circuit complexity. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the execution clusters of Jouppi in the device of Miller to increase processor parallelism and efficiency without increasing the circuit complexity.

18. Referring to claim 20, Miller in view of Jouppi has taught wherein each execution pipeline is four lanes wide and the data processor comprises three execution units (Miller column 7, line 58 to column 8, line 7; column 8, lines 8-67; column 9, line 37 to column 10, line 35; Figure 5; and Figure 6).

19. Referring to claims 21 and 22, Miller in view of Jouppi has taught each of the execution clusters comprises one or more arithmetic units, a register file, an interface to a memory controller, and an inter-cluster communication interface (Jouppi column 5, line 41 to column 6, line 28 and Figure 2B).

Response to Arguments

20. The Examiner withdraws the objections to the specification in favor of the amended specification.

21. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

22. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

23. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

26. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
30 September 2005

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